AMENDMENTS TO THE CLAIMS:

Please cancel claims 1-5 and 10, without prejudice. Kindly amend claims 6, 14-17, 19, 21-22 and 25, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claims 1-5 (canceled)

Claim 6 (currently amended): ~~The buffer circuit according to claim 1,~~ A buffer circuit having an input terminal for receiving an input signal and an output terminal for outputting an output signal, comprising:

a first transistor and a second transistor connected in series between a first power supply and a second power supply having different power supply voltages, each having a control terminal,

said first and second transistors being controlled to be on and off based on signals respectively fed to said control terminals,

a connection node between said first and second transistors being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

a control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit, and an output terminal for outputting the signal to be supplied to said control terminal of said second transistor, said control circuit performing control so that

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when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply, said second transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to be off, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from off to on, said second transistor is kept off,

wherein said control circuit further comprises:

an inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal;

a delay circuit for receiving the input signal supplied to said input terminal of said buffer circuit and outputting a delayed signal of the input signal; and

a logic circuit having two input terminals for receiving the output signal from said inverter and the output signal from said delay circuit and having an output terminal for outputting a signal at a logic level for turning on said second transistor to said control terminal of said second transistor when the signals received at said two input terminals are both at the second logic level; and

wherein

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the signal outputted from said delay circuit changes from the second logic level to the first logic level before a timing at which the input signal supplied to said input terminal of said buffer circuit changes from the first logic level to the second logic level, and

when the input signal supplied to said input terminal of said buffer circuit changes from the first logic level to the second logic level, said second transistor is set to be in an off state.

Claim 7 (original): The buffer circuit according to claim 6, wherein said delay circuit comprises a delay locked loop (DLL) circuit.

Claim 8 (original): A buffer circuit including a first buffer having an input terminal for receiving an input signal and an output terminal for outputting an inverted signal of the input signal; and

a second buffer circuit having an input terminal connected to said output terminal of said first buffer circuit, inverting the signal supplied to said input terminal and having an output terminal for outputting the inverted signal;

said first buffer circuit comprising:

a first transistor and a second transistor connected in series between a first power supply and a second power supply having different power supply voltages, each having a control terminal, said first and second transistors being controlled to be on and off based on signals respectively fed to said control terminals,

a connection node between said first transistor and said second transistor being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

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a first control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said first buffer circuit, and having an output terminal for outputting the signal to be supplied to said control terminal of said second transistor,

said first control circuit performing control so that

when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply, said second transistor is turned on to cause an output signal voltage of said output terminal of said buffer circuit to undergo a transition to the voltage of said second power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to be off, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from said off to on, said second transistor is kept off;

said second buffer circuit comprising:

a third transistor and a fourth transistor connected in series between said first power supply and said second power supply, being controlled to be on and off based on signals supplied to respective control terminals thereof,

a connection node between said third transistor and said fourth transistor being connected to said output terminal of said second buffer circuit,

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said control terminal of said third transistor being connected to said input terminal of said second buffer circuit; and

a second control circuit having at least an input terminal for receiving the output signal of said first buffer circuit supplied to said input terminal of said second buffer circuit and having an output terminal for outputting the signal to be supplied to said control terminal of said fourth transistor,

said second control circuit performing control so that

when the output signal of said first buffer circuit is at the first logic level, said fourth transistor is turned off,

when the output signal of said first buffer circuit changes from the first logic level to the second logic level, said fourth transistor is turned on to cause an output signal voltage of said output terminal of said second buffer circuit to undergo a transition to the voltage of said first power supply,

thereafter, before the output signal of said first buffer circuit undergoes a transition from the second logic level to the first logic level, said fourth transistor is set to be off, and

when the output signal of said first buffer circuit changes from the second logic level to the first logic level and said third transistor is switched from off to on, said fourth transistor is kept in off.

Claim 9 (original): A buffer circuit comprising:

first and second MOS transistors of mutually opposite conductivity types, connected in series between a high-potential power supply and a low-potential power supply,

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a connection node between a drain of said first MOS transistor and a drain of said second MOS transistor being connected to an output terminal of said buffer circuit,

a gate of said first MOS transistor being connected to an input terminal of said buffer circuit; and

a control circuit receiving an input signal supplied to said input terminal of said buffer circuit and outputting a signal to be supplied to a gate of said second MOS transistor,

said control circuit performing control so that

when the input signal is at a second logic level corresponding to a voltage of said low-potential power supply, said second MOS transistor is turned off,

when the input signal is at a first logic level corresponding to a voltage of said high-potential power supply, said second MOS transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to undergo a transition to the voltage of said low-potential power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, the signal supplied to said gate of said second MOS transistor is set at the second logic level to turn off said second MOS transistor, and

when the input signal undergoes a transition from the first logic level to the second logic level to cause said first MOS transistor to transition from off to on, said second MOS transistor is kept off.

Claim 10 (canceled)

Claim 11 (original) The buffer circuit according to claim 9, wherein said control circuit comprises:

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a first inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal; and

a logic circuit having two input terminals for receiving the output signal from said first inverter and an inverted signal of the output signal of said output terminal of said buffer circuit and having an output terminal for outputting the signal at a logic level for turning on said second MOS transistor to a control terminal of said second MOS transistor when the signals input to said two input terminals are both at the second logic level.

Claim 12 (original): The buffer circuit according to claim 9, further comprising:

a flip-flop including a second inverter having an input terminal connected to said output terminal of said buffer circuit and

a third inverter having an input terminal connected to an output terminal of said second inverter and having an output terminal connected to said output terminal of said buffer circuit;

wherein said logic circuit of said control circuit receives an output signal of said first inverter and an output signal of said second inverter at said two respective input terminal thereof.

Claim 13 (original): The buffer circuit according to claim 9, wherein said control circuit comprises:

a first inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal;

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a delay circuit receiving the input signal supplied to said input terminal of said buffer circuit and delaying the input signal to output the delayed signal; and

a logic circuit having two input terminals for receiving the output signal from said first inverter and the output signal of said delay circuit and having an output terminal for outputting a signal at a logic level for turning on said second MOS transistor to a control terminal of said second MOS transistor when the signals input to said two input terminals are both at the second logic level.

Claim 14 (currently amended): ~~The buffer circuit according to claim 1,~~ A buffer circuit having an input terminal for receiving an input signal and an output terminal for outputting an output signal, comprising:

a first transistor and a second transistor connected in series between a first power supply and a second power supply having different power supply voltages, each having a control terminal,

said first and second transistors being controlled to be on and off based on signals respectively fed to said control terminals,

a connection node between said first and second transistors being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

a control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit, and an output terminal for outputting the signal to

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be supplied to said control terminal of said second transistor, said control circuit performing control so that

when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply, said second transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to be off, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from off to on, said second transistor is kept off;

wherein said control circuit further includes an input terminal for receiving a selection control signal for controlling activation and deactivation of said buffer circuit; and

said control circuit outputting the signal at a logic level for turning off said second transistor when the selection control signal input thereto indicates a value commanding deactivation of said buffer circuit.

Claim 15 (currently amended): ~~The buffer circuit according to claim 1,~~ A buffer circuit having an input terminal for receiving an input signal and an output terminal for outputting an output signal, comprising:

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a first transistor and a second transistor connected in series between a first power supply and a second power supply having different power supply voltages, each having a control terminal,

said first and second transistors being controlled to be on and off based on signals respectively fed to said control terminals,

a connection node between said first and second transistors being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

a control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit, and an output terminal for outputting the signal to be supplied to said control terminal of said second transistor, said control circuit performing control so that

when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply, said second transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to be off, and

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when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from off to on, said second transistor is kept off,

wherein said control circuit further comprises:

a logic circuit receiving the input signal supplied to said input terminal of said buffer circuit, the output signal outputted from said output terminal of said buffer circuit, and a selection control signal for controlling activation and deactivation of said buffer circuit or an inverted signal of the selection control signal, and

generating the signal to be supplied to said control terminal of said second transistor based on a result of a logic operation on the signals received; and wherein

said logic circuit outputs the signal at a logic level for turning off said second transistor to said control terminal of said second transistor from an output terminal thereof, irrespective of values of the other two signals input to said logic circuit when the selection control signal commands deactivation of said buffer circuit,

generates the signal at a logic level for turning on said second transistor for supply to said control terminal of said second transistor when the selection control signal commands activation of said buffer circuit and the input signal supplied to said input terminal of said buffer circuit and the output signal outputted from said buffer circuit are both at the first logic level, and

generates the signal at said logic level for turning off said second transistor for supply to said control terminal of said second transistor when said second transistor is then turned on and the output signal outputted from said output terminal of said buffer circuit becomes the second logic level.

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Claim 16 (currently amended): ~~The buffer circuit according to claim 4,~~ A buffer circuit having an input terminal for receiving an input signal and an output terminal for outputting an output signal, comprising:

a first transistor and a second transistor connected in series between a first power supply and a second power supply having different power supply voltages, each having a control terminal,

said first and second transistors being controlled to be on and off based on signals respectively fed to said control terminals,

a connection node between said first and second transistors being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

a control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit, and an output terminal for outputting the signal to be supplied to said control terminal of said second transistor, said control circuit performing control so that

when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply, said second transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply,

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thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to be off, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from off to on, said second transistor is kept off further comprising a flip-flop circuit having an input terminal connected to said output terminal of said buffer circuit, for storing and holding a logic level of the output signal of said buffer circuit and having an output terminal for outputting a signal which said flip-flop circuit stores and holds, said output terminal of said flip-flop circuit being connected to said output terminal of said buffer circuit, wherein said control circuit further comprises:

an inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal; and

a logic circuit having first, second and third input terminals for receiving a signal at a logic level inverted from said logic level of the output signal of the output terminal of said buffer circuit and stored and held in said flip-flop circuit, the output signal of said inverter, and a selection control signal for controlling activation and deactivation of said buffer circuit or an inverted signal of the selection control signal respectively;

said logic circuit having an output terminal for outputting the signal at a logic level for turning on said second transistor to said control terminal of said second transistor when the selection control signal supplied to said third input terminal indicates a value commanding activation of said buffer circuit and the signals supplied to said first and second input terminals are both at the second logic level,

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said logic circuit outputting the signal at a logic level for turning off said second transistor from said output terminal thereof to said control terminal of said second transistor from said output terminal thereof, irrespective of values of the other two input signals, when the selection control signal commands deactivation of said buffer circuit.

Claim 17 (currently amended): ~~The buffer circuit according to claim 1,~~ A buffer circuit having an input terminal for receiving an input signal and an output terminal for outputting an output signal, comprising:

a first transistor and a second transistor connected in series between a first power supply and a second power supply having different power supply voltages, each having a control terminal,

said first and second transistors being controlled to be on and off based on signals respectively fed to said control terminals,

a connection node between said first and second transistors being connected to said output terminal of said buffer circuit,

said control terminal of said first transistor being connected to said input terminal of said buffer circuit; and

a control circuit having at least an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit, and an output terminal for outputting the signal to be supplied to said control terminal of said second transistor, said control circuit performing control so that

when the input signal is at a second logic level corresponding to the voltage of said second power supply, said second transistor is turned off,

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when the input signal changes from the second logic level to a first logic level corresponding to the voltage of said first power supply, said second transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to change to the voltage of said second power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level, said second transistor is set to be off, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first transistor is switched from off to on, said second transistor is kept off,

wherein said control circuit further comprises:

an inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal;

a delay circuit for receiving the input signal supplied to said input terminal of said buffer circuit and outputting a delayed signal of the input signal; and

a logic circuit having first, second and third input terminals for receiving the output signal of said inverter,

the output signal of said delay circuit, and

a selection control signal for controlling activation and deactivation of said buffer circuit or an inverted signal of selection control signal, respectively,

said logic circuit having an output terminal for outputting a signal at a logic level for turning on said second transistor to said control terminal of said second transistor when the selection control signal supplied to said third input terminal indicates a value commanding

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activation of said buffer circuit and the signals supplied to said first and second input terminals are both at the second logic level,

said logic circuit outputting a signal at a logic level for turning off said second transistor to said control terminal of said second transistor from said output terminal, irrespective of values of the signals input to said first and second input terminals, when the selection control signal commands deactivation of said buffer circuit;

wherein when said buffer circuit is activated, the signal outputted from said delay circuit changes from the second logic level to the first logic level before a timing at which the input signal supplied to said input terminal of said buffer circuit changes from the first logic level to the second logic level, and when the input signal supplied to said input terminal of said buffer circuit changes from the first logic level to the second logic level, said second transistor is set to be off.

Claim 18 (original): The buffer circuit according to claim 8, wherein said first control circuit further includes an input terminal for receiving a selection control signal for controlling activation and deactivation of said first buffer circuit, said first control circuit outputting the signal at a logic level for turning off said second transistor when the selection control signal indicates a value commanding deactivation of said first buffer circuit; and

said second control circuit further includes an input terminal for receiving a selection control signal for controlling activation and deactivation of said second buffer circuit; said second control circuit outputting the signal at a logic level for turning off said fourth transistor when the selection control signal indicates a value commanding deactivation of said second buffer circuit.

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Claim 19 (currently amended): The buffer circuit according to claim 9, wherein said control circuit comprises:

a first inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input terminal; and

a logic circuit having first, second and third input terminals for receiving the output signal of said first inverter, an inverted signal of the output signal of said output terminal of said buffer circuit, and a selection control signal for controlling activation and deactivation of said buffer circuit or an inverted signal of the selection control signal, respectively,

said logic circuit having an ~~ouput~~ output terminal for outputting the signal at a logic level for turning on said second MOS transistor to a control terminal of said second MOS transistor when the selection control signal supplied to said third input terminal commands activation of said buffer circuit and the signals supplied to said first and second input terminals are both at the second logic level,

said logic circuit outputting the signal at a logic level for turning off said second MOS transistor to said control terminal of said second MOS transistor from said output terminal thereof when the selection control signal supplied to said third input terminal commands deactivation of said buffer circuit.

Claim 20 (original): The buffer circuit according to claim 19, further comprising:

a flip-flop including a second inverter having an input terminal connected to said output terminal of said buffer circuit and

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a third inverter having an input terminal connected to an output terminal of said second inverter and an output terminal connected to said output terminal of said buffer circuit;

wherein said logic circuit of said control circuit receives the output signal of said first inverter, an output signal of said second inverter, and the selection control signal or the inverted signal thereof at said three respective input terminals.

Claim 21 (currently amended): A semiconductor integrated circuit comprising said buffer circuit as defined in claim [[1]] 9 as a clock tree buffer.

Claim 22 (currently amended): A buffer tree circuit having a plurality of buffer circuits disposed in a tree form along clock interconnection paths, including as said plurality of buffer circuits, a plurality of first and second buffer circuits as defined in claim 8, and

a plurality of the first buffer circuits cascaded alternately with a plurality of the second buffer circuits.

Claim 23 (original): The buffer circuit according to claim 10, wherein said control circuit comprises:

a first inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal; and

a logic circuit having two input terminals for receiving the output signal from said first inverter and an inverted signal of the output signal of said output terminal of said buffer circuit and having an output terminal for outputting the signal at a logic level for turning on said second MOS transistor to a control terminal of said second MOS transistor when the signals input to said two input terminals are both at the second logic level.

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Claim 24 (original): The buffer circuit according to claim 10, further comprising:

a flip-flop including a second inverter having an input terminal connected to said output terminal of said buffer circuit and

a third inverter having an input terminal connected to an output terminal of said second inverter and having an output terminal connected to said output terminal of said buffer circuit;

wherein said logic circuit of said control circuit receives an output signal of said first inverter and an output signal of said second inverter at said two respective input terminal thereof.

Claim 25 (currently amended): ~~The buffer circuit according to claim 10,~~ A buffer circuit comprising:

first and second MOS transistors of mutually opposite conductivity types, connected in series between a high-potential power supply and a low-potential power supply,

a connection node between a drain of said first MOS transistor and a drain of said second MOS transistor being connected to an output terminal of said buffer circuit,

a gate of said first MOS transistor being connected to an input terminal of said buffer circuit; and

a control circuit receiving an input signal supplied to an input terminal of said buffer circuit and outputting a signal to be supplied to a gate of said second MOS transistor,

said control circuit performing control so that

when the input signal is at a second logic level corresponding to a voltage of said high-potential power supply,

said second MOS transistor is turned off,

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when the input signal is at a first logic level corresponding to a voltage of said low-potential power supply,

said second MOS transistor is turned on to cause a voltage of an output signal of said output terminal of said buffer circuit to undergo a transition to the voltage of said high-potential power supply,

thereafter, before the input signal undergoes a transition from the first logic level to the second logic level,

the signal supplied to said gate of said second MOS transistor is set at the second logic level to turn off said second MOS transistor, and

when the input signal undergoes a transition from the first logic level to the second logic level and said first MOS transistor undergoes a transition from off to on, said second MOS transistor is kept off,

wherein said control circuit further comprises:

a first inverter having an input terminal for receiving the input signal supplied to said input terminal of said buffer circuit and an output terminal for outputting an inverted signal of the input signal;

a delay circuit receiving the input signal supplied to said input terminal of said buffer circuit and delaying the input signal to output the delayed signal; and

a logic circuit having two input terminals for receiving the output signal from said first inverter and the output signal of said delay circuit and having an output terminal for outputting a signal at a logic level for turning on said second MOS transistor to a control terminal of said

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second MOS transistor when the signals input to said two input terminals are both at the second logic level.

Claim 26 (original): A buffer circuit having at least an input terminal and an output terminal; said buffer circuit further comprising:

a pair of transistors connected to said output terminal, respectively pulling up and pulling down said output terminal based on the input signal received at said input terminal;

a control circuit, receiving at least said input signal for controlling to cause one transistor of said paired transistors which is turned on based on said input signal to be in an off state at least at a beginning of a transition of other transistor of said paired transistors switching from an off state to an on state according to a transition of said input signal.

Claim 27 (original): A buffer circuit according to claim 26, further comprising a circuit for setting and holding an output signal at said output terminal to a logic value which corresponds to a logic value at the output terminal immediately before said one transistor is caused to be turned off, during when said paired transistors are both off.

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